

WHAT IS CLAIMED IS:

1. An adaptive clock throttle for interfacing a clock generator generating a high speed clock and a processing engine operating in response to a processing clock, the adaptive clock throttle operable to:
 - generate a plurality of lower speed clocks from the high speed clock;
 - estimate a duty cycle of the processing engine; and
 - selectively gate one of the lower speed clocks to the processing engine as the processing clock to increase the duty cycle of the processing engine.
2. The adaptive clock throttle of Claim 1 further operable to selectively mask the selected lower speed clock to produce a series of non-periodic clock cycles.
3. The adaptive clock throttle of Claim 2 wherein the adaptive clock throttle is operable to mask the selected lower speed clock in predetermined pattern.
4. The adaptive clock throttle of Claim 2 wherein the adaptive clock throttle is operable to pseudorandomly mask the selected lower speed clock.

[illegible]

5. The adaptive clock throttle of Claim 1 wherein the processing engine comprises a digital signal processor.
6. The adaptive clock throttle of Claim 1 wherein at least one of the lower speed clocks is asymmetric.

7. The adaptive clock throttle of Claim 1 further operable to:
monitor the status of an output data buffer of the processing engine;
detect an underflow condition in the buffer; and
selectively gate one of the high and lower speed clocks to the processing engine to increase the processing engine operating frequency in response to the underflow condition.
8. The adaptive clock throttle of Claim 1 further operable to:
monitor the status of a data buffer of the processing engine;
detect an underflow condition in the buffer; and
selectively remask the selected lower speed clock to increase the processing engine operating frequency in response to the underflow condition.

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- Figure 1 consists of 12 scatter plots, labeled (a) through (l), arranged vertically. Each plot shows the relationship between a specific variable on the x-axis and the 'Number of children per woman' on the y-axis. The variables are: (a) Age at first birth, (b) Age at last birth, (c) Age at last birth squared, (d) Age at last birth cubed, (e) Age at last birth to the power of 4, (f) Age at last birth to the power of 5, (g) Age at last birth to the power of 6, (h) Age at last birth to the power of 7, (i) Age at last birth to the power of 8, (j) Age at last birth to the power of 9, (k) Age at last birth to the power of 10, and (l) Age at last birth to the power of 11. Each plot includes a scatter of data points and a fitted curve. The curves show a positive correlation between the variable and the number of children per woman, with the strength of the correlation increasing as the power of the age variable increases.

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15. The method of Claim 14 wherein said step of detecting a data underflow condition comprises the substep of monitoring a dipstick associated with a data buffer in the processor.

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16. An audio decoder for operating on audio data received in blocks comprising:

a digital signal processor for processing blocks of audio data in response to a set of instructions;

clock generation circuitry operable to generate a plurality of clocks; and

an adaptive clock throttle interfacing the digital signal processor and the clock generation circuitry operable to:

estimate the loading on the digital signal processor as the processor executes instructions to process the blocks of audio data; and

selectively gate one of the plurality of clocks to the processor as a function of the estimated loading for timing processor operations, the clock selected to distribute the execution of instructions for a selected block of audio data across a period of the selected block.

17. The audio decoder of Claim 16 wherein the digital signal processor is a selected one of a plurality of digital signal processors integrated on a single-chip.

18. The audio decoder of Claim 16 wherein the adaptive clock throttle is further operable to selectively mask periods of the selected clock to change a frequency of the selected clock.

19. The audio decoder of Claim 16 wherein the clock generator is operable to generate at least one of the plurality of clocks as an asymmetric clock.

20. The audio decoder of Claim 16 wherein the clock generator is operable to generate the plurality of clocks from a high speed clock.